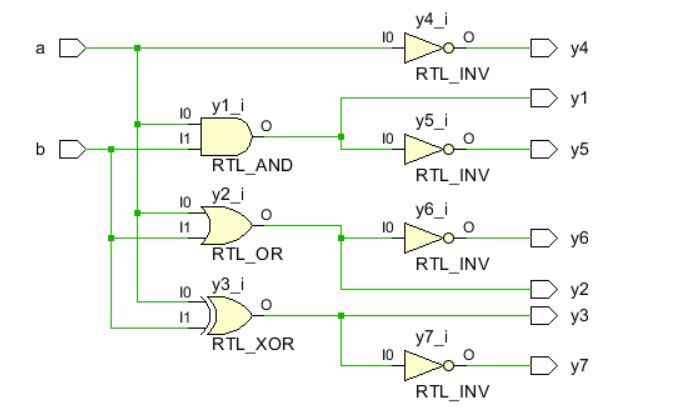
**Practical 1**

**Aim**: Write a VHDL code to implement basic gates.

|  |
| --- |
| **Code:**  library IEEE;  use IEEE.STD\_LOGIC\_1164.ALL;  entity basic\_gates is  Port ( a : in STD\_LOGIC;  b : in STD\_LOGIC;  y1 : out STD\_LOGIC;  y2 : out STD\_LOGIC;  y3 : out STD\_LOGIC;  y4 : out STD\_LOGIC;  y5 : out STD\_LOGIC;  y6 : out STD\_LOGIC;  y7 : out STD\_LOGIC);  end basic\_gates;  architecture Behavioral of basic\_gates is  begin  y1<= a and b;  y2<= a or b;  y3<= a xor b;  y4<= not a;  y5<= not ( a and b);  y6<= not ( a or b);  y7<= not ( a xor b);  end Behavioral; |

**** **RTL DIAGRAM:**

**Test bench Code :**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity Tb\_basic\_gates is

-- Port ( );

end Tb\_basic\_gates;

architecture Behavioral of Tb\_basic\_gates is

component basic\_gates is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

y1 : out STD\_LOGIC;

y2 : out STD\_LOGIC;

y3 : out STD\_LOGIC;

y4 : out STD\_LOGIC;

y5 : out STD\_LOGIC;

y6 : out STD\_LOGIC;

y7 : out STD\_LOGIC);

end component basic\_gates;

signal a,b,y1,y2,y3,y4,y5,y6,y7:std\_logic;

begin

x1:basic\_gates port map(a,b,y1,y2,y3,y4,y5,y6,y7);

process

begin

a<='0';

b<='0';

wait for 10ns;

a<='1';

b<='0';

wait for 10ns;

a<='0';

b<='1';

wait for 10ns;

a<='1';

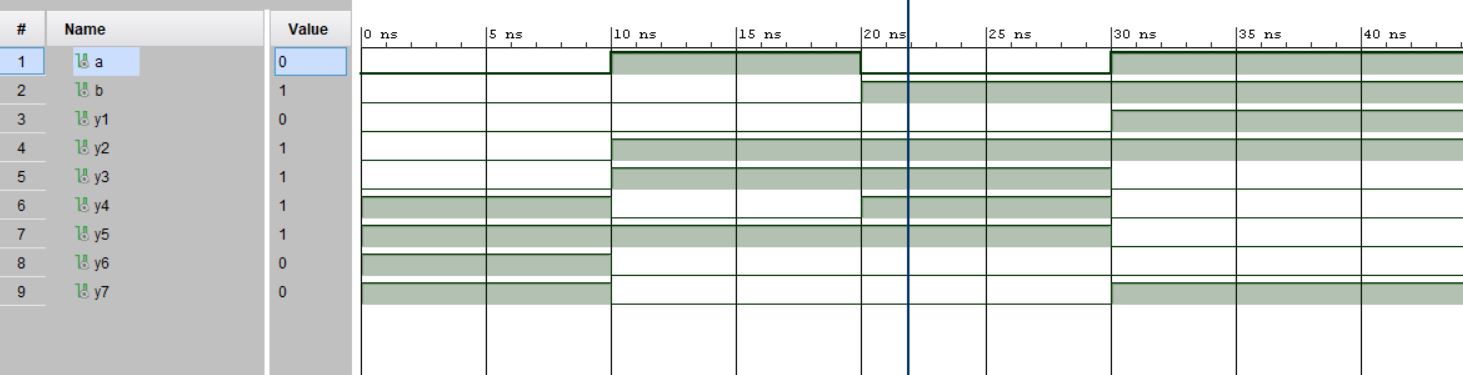
b<='1';

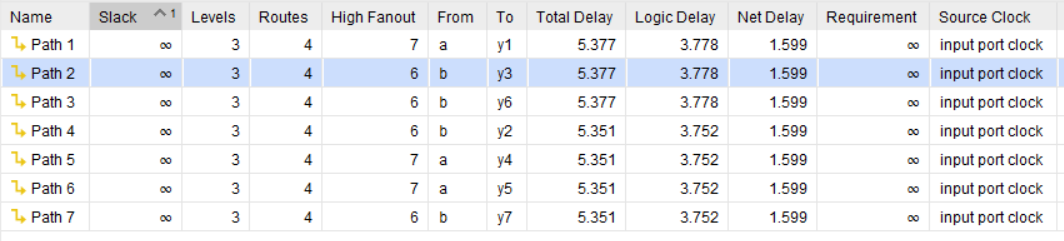
wait;

end process;

end Behavioral;

**SIMULATION WAVEFORM :**

****



**SYNTHESIS SUMMARY:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Resource** | **Utilization** | **Available** | **Utilization %** |
| LUT | 4 | 17600 | 0.02 |
| IO | 9 | 100 | 9.00 |

Maximum Combinational Delay: 5.377nSec